**NIKITA J**

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**Career objective:**

To build career in the growing organisation, where I get opportunities to prove my abilities by accepting challenges, fulfilling the organisational goal and climb the career ladder.

**Internship:**

1. Physical design Training at SOCDV worked on Physical design at Block level for 14nm technology.

**Technical Skills :**

a) Excellent in Unix commands/Used gvim commands in PD flow

b) Worked on TCl for PD applications

c) Worked in ASIC design flow (RTL to GDSII). Understanding of inputs and outputs of allthe stages involved in physical design flow (APR).

d) Implementation of congestion driven macro placement during Floor planning, Power planning with IR drop, placement, CTS and routing.

e) Analysed the complex timing reports and met timing closure on DSM technology.

f) Identifying and constraining timing paths, analyzing timing under various PVT corners, OCV, False Paths, Half cycle paths, MCMM, and CRPR.

e) Effect of Crosstalk, Electromigration, Antenna effect, Latch up and ESD for design.

f) Solved DRC, DFM, LVS .

g) Theory knowledge of SRAM bit cell and basic architecture.

Scripting: fixing violation through Tcl scripts.

h) Aware of different files: .Lib, DEF, LEF, SDC and SPEF, .tf.

i) Expertise knowledge on CMOS theory, MOSFET’s and Logic Design.

**Tools Used :**

**Synthesis :** Design Compiler

**PnR :** ICC2

**STA :** Prime Time

**Training Project:**

**Title :** ORCA\_TOP(Multi voltage) (Block level)

**Hard Macro :** 40

**I/O Ports :** 240

**Number of Clocks :** 4(2 Main clock, 1 Generated Clock and 1 virtual clock)

**Process Technology :** 28/14nm, 9 routing Layers

**Complexity :** 52047 gates

**Number of Power Domains** : 2

**Summary :**

a) Imported design using NDM methods

b) Performed sanity checks

c) Performed different iteration for creating core area and diearea

d) Written TCL script for port placement based locations

e) Placed macros according to guidelines to meet timing and to reduce congestion

f) Understood UPF and created voltage area for power domains

g) Done power planning and fixed issues after power planning

h) Done Placement and CTS with minimum congestion and timing violations

i) Done routing and fixed shorts and DRC violations after routing

j) Performed signoff RC extraction and closed timing using Prime time

k) Performed timing ECO in ICC2

**Educational Qualification :**

1. **BE**

**College/University :**Tontadarya College of Engineering Gadag

**Passout year :** 2022

**Aggregate Marks :** 8.42 cgpa

1. **PUC**

**College/University :** Tungal Science PU Composite College

**Passout year :** 2018

**Aggregate Marks :** 75.66%

1. **SSLC**

**College/University :**  C K Chinchali School

**Passout year :** 2016

**Aggregate Marks :** 91.04%

**Soft Skills:**

* Positive Attitude.
* Punctual and disciplined.
* Active learner and go-getter.
* Interactive and co-operative nature.
* Comphrensive problem solving ability, willingness to learn and good as a team player.

**Personal Details:**

Date Of Birth : 25-09-2000

Languages : Kannada,English,Hindi

Hobbies : listening music

like to cook.

**Course Certificate**

